IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A data processing apparatus comprising:

an operation processing unit connected to a data bus and configured to perform a read cycle by outputting a read control signal to a memory to read a read data word output by said memory to said data bus, and a write cycle by outputting a write control signal to said memory and a write data word to said data bus to write said write data word in the memory; and

a pseudo-data generating circuit connected to said data bus, said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit, said pseudo-data generating circuit configured to generate pseudo-data and output the generated pseudo-data to said data bus according to an output timing based on said read control signal and said write control signal output from said operation processing unit,

the output timing controlled to ~~occur~~ cause the pseudo-data generating circuit to output the generated pseudo-data between a read cycle and an immediately following write cycle, between a write cycle and an immediately following read cycle, between a read cycle and an immediately following read cycle, or between a write cycle and an immediately following write cycle, and

the output timing controlled to prevent the pseudo-data generating circuit from outputting the generated pseudo-data during the read cycle and the immediately following write cycle, during the write cycle and the immediately following read cycle, during the read cycle and the immediately following read cycle, or during the write cycle and the immediately following write cycle.

Claim 2 (Original): The data processing apparatus according to claim 1, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claim 3 (Currently Amended): A data processing apparatus comprising:

an operation processing unit configured to perform an operation processing and output a read signal and a write signal;

a data bus connected to said operation processing unit;

a memory configured to receive the read signal and the write signal from the operation processing unit and configured to output a read data on the data bus in response to the read signal, and store a write data from the data bus in response to the write signal;

a control signal generating circuit configured to receive said read signal and said write signal from the operation processing unit, detect a change in the read signal ~~or~~ and a change in the write signal, and generate a control signal based on the detected change; and

a pseudo-data generating circuit connected to said data bus and configured to receive the control signal from the control signal generating circuit, generate pseudo-data, and output the generated pseudo-data to said data bus in accordance with a timing of the control signal.

Claim 4 (Original): The data processing apparatus according to claim 3, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claims 5-10 (Canceled).

Claim 11 (Currently Amended): A memory card comprising:

an operation processing unit connected to a data bus and configured to perform a read cycle by outputting a read control signal to a memory to read a read data word output by said

memory to said data bus, and a write cycle by outputting a write control signal to said memory and a write data word to said data bus to write said write data word in the memory;

an input/output circuit connected to said data bus, said input/output circuit configured to input external data onto said data bus and output data on said data bus to an external apparatus; and

a pseudo-data generating circuit connected to said data bus, said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit, said pseudo-data generating circuit configured to generate pseudo-data and output the generated pseudo-data to said data bus according to an output timing based on said read control signal and said write control signal output from said operation processing unit,

the output timing controlled to ~~occur~~ cause the pseudo-data generating circuit to output the generated pseudo-data between a read cycle and an immediately following write cycle, between a write cycle and an immediately following read cycle, between a read cycle and an immediately following read cycle, or between a write cycle and an immediately following write cycle, and

the output timing controlled to prevent the pseudo-data generating circuit from outputting the generated pseudo-data during the read cycle and the immediately following write cycle, during the write cycle and the immediately following read cycle, during the read cycle and the immediately following read cycle, or during the write cycle and the immediately following write cycle.

Claim 12 (Original): The memory card according to claim 11, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claim 13 (Currently Amended): A memory card comprising:

an operation processing unit configured to perform an operation processing and output a read signal and a write signal;

a data bus connected to said operation processing unit;

an input/output circuit connected to said data bus, said input/output circuit configured to input external data onto said data bus and output data on said data bus to an external apparatus;

a memory configured to receive the read signal and the write signal from the operation processing unit and configured to output a read data on the data bus in response to the read signal, and store a write data from the data bus in response to the write signal;

a control signal generating circuit configured to receive said read signal and said write signal from the operation processing unit, detect a change in the read signal ~~or~~ and a change in the write signal, and generate a control signal based on the detected change; and

a pseudo-data generating circuit connected to said data bus and configured to receive the control signal from the control signal generating circuit, generate pseudo-data, and output the generated pseudo-data to said data bus in accordance with a timing of the control signal.

Claim 14 (Original): The memory card according to claim 13, wherein said pseudo-data generating circuit generates random number data as the pseudo-data.

Claim 15 (Previously Presented): The apparatus of claim 1, wherein:

the operation processing unit is further configured to output the read control signal to have an active read control time period and an inactive read control time period, and output the write control signal to have an active write control time period and an inactive write control time period, and

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to prevent the output of the generated pseudo-data to the data bus during at least one of the active read control time period and the active write control time period.

Claim 16 (Previously Presented): The apparatus of claim 15, wherein:

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period.

Claim 17 (Previously Presented): The apparatus of claim 3, wherein:

the operation processing unit is further configured to output the read signal to have an active read signal time period and an inactive read signal time period, and output the write signal to have an active write signal time period and an inactive write signal time period, and

the control signal generating circuit is further configured to control an output timing of the control signal to prevent the output of the generated pseudo-data to the data bus during at least one of the active read signal time period and the active write signal time period.

Claim 18 (Previously Presented): The apparatus of claim 17, wherein:

the control signal generating circuit is further configured to control the output timing of the control signal to delay the output of the generated pseudo-data by a predetermined time from at least one of the active read signal time period and the active write signal time period.

Claim 19 (Previously Presented): The memory card of claim 11, wherein:

the operation processing unit is further configured to output the read control signal to have an active read control time period and an inactive read control time period, and output the write control signal to have an active write control time period and an inactive write control time period, and

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to prevent the output of the generated pseudo-data to the data bus during at least one of the active read control time period and the active write control time period.

Claim 20 (Previously Presented): The memory card of claim 19, wherein:

the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period.

Claim 21 (Previously Presented): The memory card of claim 13, wherein:

the operation processing unit is further configured to output the read signal to have an active read signal time period and an inactive read signal time period, and output the write signal to have an active write signal time period and an inactive write signal time period, and

the control signal generating circuit is further configured to control an output timing of the control signal to prevent the output of the generated pseudo-data to the data bus during at least one of the active read signal time period and the active write signal time period.

Claim 22 (Previously Presented): The memory card of claim 21, wherein:

the control signal generating circuit is further configured to control the output timing of the control signal to delay the output of the generated pseudo-data by a predetermined time from at least one of the active read signal time period and the active write signal time period.

Claim 23 (New): The apparatus of claim 16, wherein the predetermined time period is shorter than the active read control time period or the active write control time period.

Claim 24 (New): The apparatus of claim 18, wherein the predetermined time period is shorter than the active read control time period or the active write control time period.

Claim 25 (New): The memory of claim 20, wherein the predetermined time period is shorter than the active read control time period or the active write control time period.

Claim 26 (New): The memory of claim 22, wherein the predetermined time period is shorter than the active read control time period or the active write control time period.

Claim 27 (New): A data processing apparatus comprising:

an operation processing unit connected to a data bus and configured to perform a read cycle by outputting a read control signal to a memory to read a read data word output by said memory to said data bus, and a write cycle by outputting a write control signal to said memory and a write data word to said data bus to write said write data word in the memory; and

a dummy circuit connected to said data bus, said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit, said dummy circuit configured to consume power and not consume power according to

an output timing based on said read control signal and said write control signal output from said operation processing unit,

the output timing controlled to cause the dummy circuit to consume power between a read cycle and an immediately following write cycle, between a write cycle and an immediately following read cycle, between a read cycle and an immediately following read cycle, or between a write cycle and an immediately following write cycle, and

the output timing controlled to cause the dummy circuit not to consume power during the read cycle and the immediately following write cycle, during the write cycle and the immediately following read cycle, during the read cycle and the immediately following read cycle, or during the write cycle and the immediately following write cycle.

Claim 28 (New): A data processing apparatus comprising:

an operation processing unit configured to perform an operation processing and output a read signal and a write signal;

a data bus connected to said operation processing unit;

a memory configured to receive the read signal and the write signal from the operation processing unit and configured to output a read data on the data bus in response to the read signal, and store a write data from the data bus in response to the write signal;

a control signal generating circuit configured to receive said read signal and said write signal from the operation processing unit, detect a change in the read signal and a change in the write signal, and generate a control signal based on the detected change; and

a dummy circuit connected to said data bus and configured to receive the control signal from the control signal generating circuit, consume power, and not consume power in accordance with a timing of the control signal.